About this Manual

We've added this manual to the Agilent website in an effort to help you support your product. This manual is the best copy we could find; it may be incomplete or contain dated information. If we find a more recent copy in the future, we will add it to the Agilent website.

Support for Your Product

Agilent no longer sells or supports this product. Our service centers may be able to perform calibration if no repair parts are needed, but no other support from Agilent is available. You will find any other available product information on the Agilent Test & Measurement website, www.tm.agilent.com.

HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. In other documentation, to reduce potential confusion, the only change to product numbers and names has been in the company name prefix: where a product number/name was HP XXXX the current name/number is now Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

Your Comments Please

HP E2444A

Your comments assist us in meeting your needs better. Please complete this questionnaire and return it to us. Feel free to add any additional comments that you might have. All comments and suggestions become the property of Hewlett-Packard. Omit any questions that you feel would be proprietary.

	Yes	No
1. Did you receive your product when expected?	[ ]	[ ]
2. Were you satisfied with the operation of the preprocessor interface at turn-on?	[ ]	[ ]

3. Were the proper accessories supplied with your product?

   If not, what was missing?

   Cables [ ] Manual(s) [ ] Other _____

4. What measurements will this preprocessor interface be used to make?

   _____

5. Which logic analyzer are you using?

   Type _____

6. What do you like most about the preprocessor interface?

   _____

7. What would you like to see changed or improved? _____

8. Which sections of the manual(s) have you used?

   [ ] Installation Overview
   [ ] Step-By-Step Procedures
   [ ] Specifications
   [ ] Schematics and Parts List

9. Please rate the manual(s) on the following:

   4= Excellent 3= Good 2= Adequate 1= Poor

   [ ] Breadth and depth of information
   [ ] Ability to easily find information
   [ ] Ability to understand and apply the information provided in the manual

   Please explain: _____

10. What is your experience with logic analyzers and preprocessor interfaces?

    [ ] No previous experience
    [ ] Less than 1 year experience
    [ ] More than 1 year's experience on one model
    [ ] More than 1 year's experience on several models

Name _____ Company _____

Address _____ Zip Code _____

Phone _____ Instrument Serial # _____

THANK YOU FOR YOUR HELP

NO POSTAGE NECESSARY IF MAILED IN U.S.A.

HP E2444A 80386DX/DXL Preprocessor Interface User's Guide

for the HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D, HP 16542A, and HP 16550A Logic Analyzers

Manual Part Number E2444-90902 Printed in U.S.A. April 1993
Microfiche Part Number E2444-90802

Printing History

New editions are complete revisions of the manual. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by the customer. The dates on the title page change only when a new edition is published.

A software code may be printed before the date; this indicates the version of the software product at the time the manual or update was issued. Many product updates and fixes do not require manual changes and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one to one correspondence between product updates and manual updates.

Edition 1 April 1993 E2444-90902

List of Effective Pages

The List of Effective Pages gives the date of the current edition and of any pages changed in updates to that edition. Within the manual, any page changed since the last edition is indicated by printing the date the changes were made on the bottom of the page. If an update is incorporated when a new edition of the manual is printed, the change dates are removed from the bottom of the pages and the new edition date is listed in the Printing History and on the title page.

Pages	**Effective Date**

Product Warranty

This Hewlett-Packard product has a warranty against defects in material and workmanship for a period of 1 year from date of shipment. During warranty period, Hewlett-Packard Company will, at its option, either repair or replace products that prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by Hewlett-Packard. However, warranty service for products installed by Hewlett-Packard and certain other products designated by Hewlett-Packard will be performed at Buyer's facility at no charge within the Hewlett-Packard service travel area. Outside Hewlett-Packard service travel areas, warranty service will be performed at Buyer's facility only upon Hewlett-Packard's prior agreement and Buyer shall pay Hewlett-Packard's round trip travel expenses.

For products returned to Hewlett-Packard for warranty service, the Buyer shall prepay shipping charges to Hewlett-Packard and Hewlett-Packard shall pay shipping charges to return the product to the Buyer. However, the Buyer shall pay all shipping charges, duties, and taxes for products returned to Hewlett-Packard from another country.

Hewlett-Packard warrants that its software and firmware designated by Hewlett-Packard for use with an instrument will execute its programming instructions when properly installed on that instrument.

Hewlett-Packard does not warrant that the operation of the instrument, software, or firmware will be uninterrupted or error-free.

Limitation of Warranty

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by the Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HEWLETT-PACKARD SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

Exclusive Remedies

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HEWLETT-PACKARD SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

Assistance

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For assistance, contact your nearest Hewlett-Packard Sales and Service Office.

Certification

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

Safety

This product has been designed and tested according to International Safety Requirements. To ensure safe operation and to keep the product safe, the information, cautions, and warnings in this user's guide must be heeded.

Contents

Introduction

Logic Analyzer Software Requirement
Logic Analyzers Supported
How to Use This Manual

Chapter 1: Setting Up the HP E2444A

Introduction 1-1
Duplicating the Master Disk 1-1
Equipment Supplied 1-2
Equipment Required 1-2
Installation Overview. 1-3
J2 Jumper and J3 Connector 1-4
The State/Timing Jumper (J2) 1-4
J3 Connector 1-4
Connecting to the Target System. 1-6
Connecting to the HP E2444A. 1-7
Power Up / Down Sequence 1-7
Setting Up the Analyzer from the Disk. 1-11

Chapter 2: Analyzing the Intel 80386DX/DXL

Introduction 2-1
Format Specification 2-1
Symbols 2-4
Listing Menu 2-8
The 80386DX/DXL Inverse Assemblers 2-10
Synchronizing the Inverse Assemblers. 2-11
Interpreting Data 2-13
Error Messages. 2-15
Instruction Decoding (-/?). 2-16
Coprocessor Support 2-16
Additional Information on Instruction Decoding 2-17
The IA386E Inverse Assembler. 2-18
Show/Suppress 2-19
Code Synchronization 2-19
IDT Description 2-19
Timing Analysis 2-20
Timing Format Specification 2-21

Waveform Menu 2-22
State-Per-Clock Mode 2-22

Chapter 3: General Information

Preprocessor Interface Characteristics. 3-1
Preprocessor Interface Description 3-2
80386DX/DXL Signal to HP E2444A Connector Mapping 3-6
Servicing 3-10
Dimensions. 3-10

Appendix A: Troubleshooting

Target Board Will Not Bootup A-1
"Slow or Missing Clock". A-1
Slow Clock. A-2
"No Configuration File Loaded". A-2
"Selected File is Incompatible" A-2
". . . Inverse Assembler Not Found" A-3
No Inverse Assembly A-3
Incorrect Inverse Assembly. A-3
No Activity on Activity Indicators A-3
Capacitive Loading. A-3
"State Clock Violates Overdrive Specification" A-4
Unwanted Triggers. A-4
"Waiting for Trigger" A-4
Intermittent Data Errors A-4
Bent Pins A-4
"Time from Arm Greater Than 41.93 ms.". A-5
No Setup/Hold Field on Format Screen A-5
"Default Calibration Factors Loaded" (16540/41/42). A-5

Introduction

The HP E2444A Preprocessor Interface provides a complete interface between any 80386DX/DXL target system and the following logic analyzers: HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D, HP 16542A, or HP 16550A.

The 80386DX/DXL configuration software on the flexible disk sets up the format specification menu of the logic analyzer for compatibility with the 80386DX/DXL microprocessors. It also loads the inverse assembler for obtaining displays of 80386DX/DXL data in 80386DX/DXL assembly language mnemonics.

Logic Analyzer Software Requirement

The HP E2444A Preprocessor Interface requires HP 16500A system and module software version V05.03 or higher (HP 16540/16541A,D HP 16542A, and HP 16550A Logic Analyzers). For the HP 16500B mainframe, system and module software version V01.00 or higher is required. For the HP 1660A/61A Logic Analyzers, software version V01.00 or higher is required. To use the enhanced inverse assembler with the HP 1660A/61A Logic Analyzers, software version V02.00 or higher is required. If your software version is older than those listed above, load new system software with the above version numbers or higher before loading the HP E2444A software.

Logic Analyzers Supported

The following logic analyzers are supported by the HP E2444A Preprocessor Interface:

HP 1650A, HP 1650B, HP 16510A, HP 16510B, and HP 1652B

These logic analyzers provide 1 k of memory depth with either 80 channels of 35 MHz state analysis (25 MHz state analysis for the HP 1650A or HP 16510A) or 80 channels of 100 MHz timing analysis.

HP 16511B

This logic analyzer combination provides 1 k of memory depth with either 160 channels of 35 MHz state analysis or 80 channels of 35 MHz state analysis and 80 channels of 100 MHz timing analysis.

HP 1660A/61A

The HP 1660A/61A Logic Analyzers provide 4 k of memory depth with 136 channels (HP 1660A) or 102 channels (HP 1661A) of 100 MHz state analysis or 250 MHz timing analysis. These logic analyzers also support various combinations of mixed state/timing analysis.

HP 16540A,D with one or two HP 16541A,D Expansion Cards

This logic analyzer combination provides 4 k of memory depth (16 k with the D version) with up to either 64 or 112 channels of 100 MHz state or timing analysis.

HP 16542A (Master Card and four expansion cards)

This logic analyzer combination provides 1 M of memory depth with 80 channels of 100 MHz state or timing analysis.

HP 16550A

This logic analyzer provides 4 k of memory depth with 102 channels per card of 100 MHz state analysis or 250 MHz timing analysis. The logic analyzer will also support various combinations of mixed state/timing analysis.

How to Use This Manual

This manual is organized into three chapters and one appendix:

- Chapter 1 explains how to install and configure the HP E2444A Preprocessor Interface for state and timing analysis with the supported logic analyzers.
- Chapter 2 provides reference information on the format specification and symbols configured by the HP E2444A software. It also provides information about the inverse assembler and status encoding.
- Chapter 3 contains additional reference information including the characteristics and signal mapping for the HP E2444A Preprocessor Interface. It also contains information on servicing.
- Appendix A contains information on troubleshooting problems or difficulties which may occur with the preprocessor interface.

1

Setting Up the HP E2444A

Introduction

The HP E2444A Preprocessor Interface provides a complete interface between an 80386DX/DXL target system and the following HP logic analyzers: HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A, HP 16510A, HP 16510B, HP 16511B, HP 16540A,D with two HP 16541A,D Expansion Cards, HP 16542A (Master Card and four expansion cards), or HP 16550A. The preprocessor interface connects the signals from the 80386DX/DXL target microprocessor to the logic analyzer inputs, and generates all status and clock signals required by the software for inverse assembly of the 80386DX/DXL instruction set.

The 80386DX/DXL Preprocessor Interface operates in the bus mode. In the bus mode all bus cycles, including prefetches, are sent to the logic analyzer as they occur. All coprocessor cycles on the local bus are also captured.

The 80386DX/DXL configuration software on the flexible disk sets up the format specification of the logic analyzer for compatibility with the 80386DX/DXL microprocessor. It also loads the inverse assembler routine for obtaining displays of 80386DX/DXL data in assembly language mnemonics.

The preprocessor interface can be used for timing analysis as well as state analysis. The State/Timing jumper on the preprocessor interface board determines which type analysis is obtained. In the Timing position, a minimal amount of skew is added between the signals.

Duplicating the Master Disk

Before you use the HP E2444A software, use the Duplicate Disk operation in the disk menu of your logic analyzer to make a duplicate copy of the HP E2444A master disk. Store the master disk and use the back-up copy to configure your logic analyzer. This will help prevent the possibility of losing or destroying the original files in the event the disk wears out, is damaged, or a file is accidentally deleted.

Equipment Supplied

The HP E2444A Preprocessor Interface consists of the following equipment:

- The preprocessor interface hardware, which includes the preprocessor interface circuit card and cable assembly.
- The inverse assembly software on a 3.5-inch disk.
- This user's guide.

Note

The preprocessor interface socket assembly pins are covered at the time of shipment with either a conductive foam wafer or a conductive plastic pin protector. This is done to protect the delicate gold-plated pins of the assembly from damage due to impact. When you're not using the preprocessor interface, protect the socket assembly pins from damage by covering them with the foam or plastic pin protector.

Equipment Required

The minimum hardware required for analysis of an 80386DX/DXL target system consists of the following equipment:

- An HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A, HP 16510A, HP 16510B, HP 16511B, HP 16540A,D with two HP 16541A,D Expansion Cards, HP 16542A (Master Card and four expansion cards), or HP 16550A.
- The 80386DX/DXL Preprocessor Interface and Inverse Assembler (HP E2444A).

Installation Overview

The following procedure describes the major steps required to perform measurements with the HP E2444A Preprocessor Interface. The page numbers listed in the various steps refer you to sections in the manual that offer more detailed information.

Caution 

To prevent equipment damage, remove the power from both the logic analyzer and the target system whenever the preprocessor interface or microprocessor is being connected or disconnected.

1. Ensure the State/Timing jumper is configured appropriately for state or timing analysis (see page 1-4).
2. Connect the 80386DX/DXL preprocessor interface to the target system (see page 1-6).
3. Plug the logic analyzer cables into the preprocessor interface pods as listed in table 1-1 (see page 1-7).
4. Load the logic analyzer configuration and inverse assembler for the specified logic analyzer (see page 1-11).
5. For timing analysis, select the configuration menu of the logic analyzer and select Timing as the analyzer 'Type" (see page 2-20).

J2 Jumper and J3 Connector

There is one jumper and one additional connector on the HP E2444A, J2 and J3 (see figure 1-1). J2 is the State/Timing jumper. J3 contains additional signals which can be monitored with the General Purpose (GP) Probes supplied with your logic analyzer.

The State/Timing Jumper (J2)

The State/Timing jumper allows you to configure the HP E2444A preprocessor interface for either state or timing analysis. For state analysis, this jumper must be open (jumper removed); for timing analysis, the circuit must be closed (jumper installed).

When the J2 jumper is in place (closed), the buffers on the preprocessor interface are flow-through buffers, adding only minimal skew to signals. When the jumper is removed, the buffers behave as latches, which capture and hold data based on the assertion of ADS and READY.

A31 - 2 and D31 - 0 are latched address and data when the jumper is open. In State-Per-Clock mode, it is best to close the jumper J2 so that the buffers are flow through, and all signals sampled are relative to each other. If you use State-Per-Clock mode with J2 open, valid address and data appear two states after ADS and READY are asserted, respectively.

J3 Connector

The J3 connector contains the HOLD, INTR, and NMI signals (see figure 1-1). To view these signals, use the GP probes supplied with your logic analyzer, and connect these signals to an unused logic analyzer pod. Note that a signal ground connection is not provided or required, since the logic analyzer is already grounded when the other pods are connected.

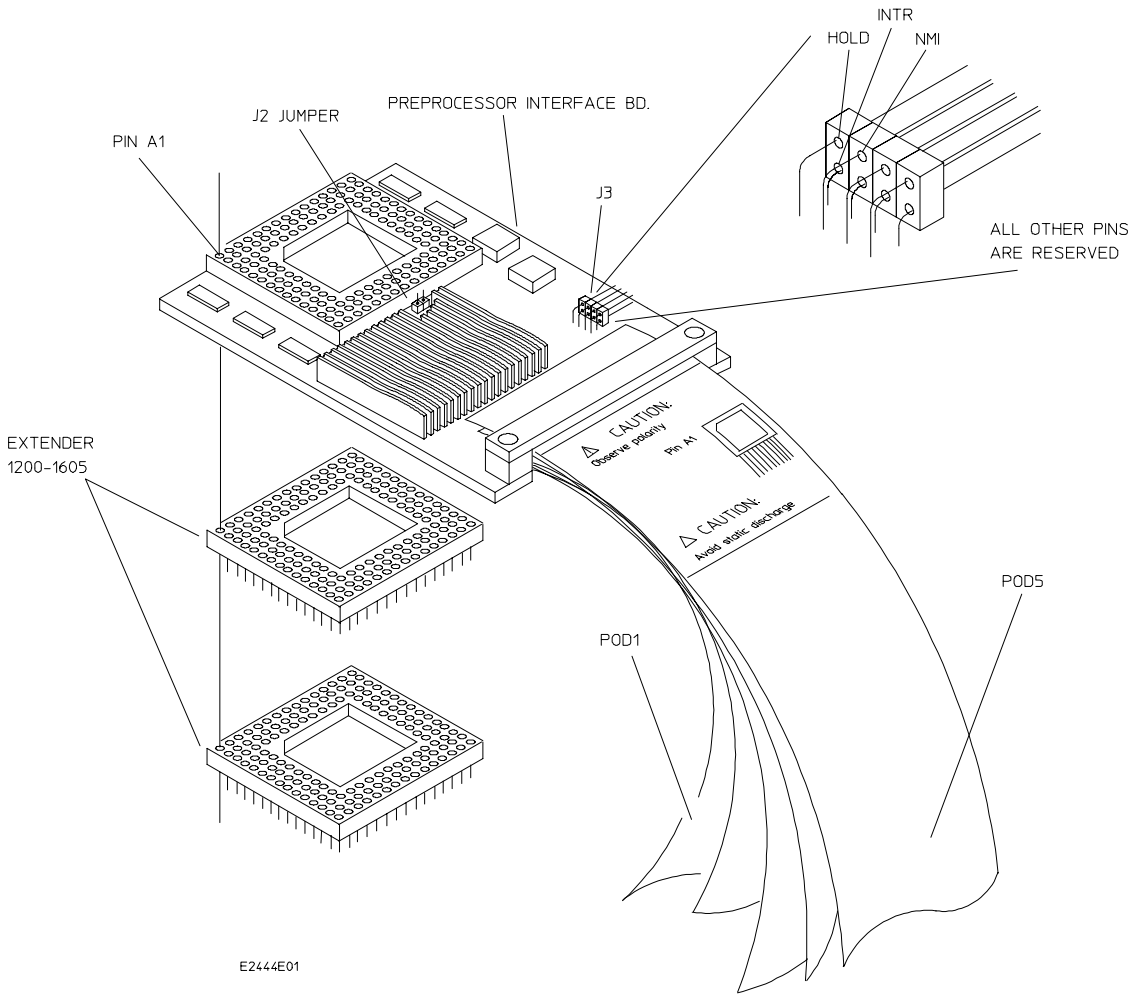

Figure 1-1. HP E2444A Preprocessor Interface

Connecting to the Target System

The following steps explain how to connect the HP E2444A Preprocessor Interface to your target system:

Caution

To prevent equipment damage, be sure to remove power from both the logic analyzer and the target system whenever the preprocessor interface or microprocessor is being connected or disconnected.

1. Remove the 80386 microprocessor from its socket on the target system and store it in a protected environment.

Caution

Serious damage to the target system or preprocessor interface can result from incorrect connection. Note the position of pin A1 (figure 1-1) on the preprocessor interface connector and the target system socket prior to inserting the connector in the socket. Also, take care to align the preprocessor interface connector with the socket on the target system so that all microprocessor pins are making contact.

2. Plug the preprocessor interface connector into the microprocessor socket on the target system.

Note

If the preprocessor interface connector interferes with components of the target system or if a higher profile is required, additional plastic pin protectors/extenders can be added. Plastic pin protectors/extenders can be ordered from Hewlett-Packard using the part number 1200-1605. However, any 132-pin PGA IC socket with an 80386 footprint and gold-plated pins can be used.

3. Plug the 80386 microprocessor into the socket on the preprocessor interface board. The socket on the preprocessor interface board is designed with low-insertion-force pins to allow you to install or remove the microprocessor with minimum force.
4. Apply power to the logic analyzer first, and then to your target system. The logic analyzer must be powered up first, since it supplies power to the preprocessor interface.

Connecting to the HP E2444A

Connect the logic analyzer cables to the preprocessor interface as shown in table 1-1 (following pages). Designations such as P1 refer to connectors on the preprocessor interface, while Pod 1 refers to a logic analyzer pod.

Figure 1-2 (page 1-10) shows the relative locations for the logic analyzer cards.

Power Up / Down Sequence

When powering up, the logic analyzer must be powered up first, and then the target system. The logic analyzer provides the power to the active circuits on the preprocessor interface; unpowered circuits may cause improper operation of the target system.

When powering down, the target system should be powered down first, and then the logic analyzer.

Table 1-1. Logic Analyzer Connections and Configuration Files
(HP 1650/60 series, HP 16510A/B, HP 16511B, HP 16540/16541A,D, HP 16550A)

Logic Analyzer	File	Pod 7	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP 1650A/B, HP 1652B, and HP 16510A/B	PI386_01		P5 (STAT)	P4 (ADDR)	P3 (ADDR)	P2 (DATA)	P1 (DATA) clk ↑
HP 16511B Upper (Master) Card	PI386_02		--	--	--	--	--
HP 16511B Lower (Expander) Card			P5 (STAT)	P4 (ADDR)	P3 (ADDR)	P2 (DATA)	P1 (DATA) clk ↑
HP 16541A,D Expansion Card 1	PI386_03				P5 (STAT)	P4 (ADDR)	P3 (ADDR)
HP 16540A,D Master Card							P1 (DATA) clk ↑
HP 16541A,D Expansion Card 2					--	--	P2 (DATA)
HP 16550A, HP 1661A	PI386_04	--	P5 (STAT)	P4 (ADDR)	P3 (ADDR)	P2 (DATA)	P1 (DATA) clk ↑
HP 1660A	PI386_04	**(Pod 7)** P5 (STAT)	--	P4 (ADDR)	P3 (ADDR)	P2 (DATA)	P1 (DATA) clk ↑

Table 1-1. Logic Analyzer Connections and Configuration Files (HP 16542A)

Logic Analyzer	File	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP 16542A Expansion Card 1	PI386_03						P5 (STAT)
HP 16542A Expansion Card 2							P4 (ADDR)
HP 16542A Master Card							P1 (DATA) clk ↑
HP 16542A Expansion Card 3							P3 (ADDR)
HP 16542A Expansion Card 4							P2 (DATA)

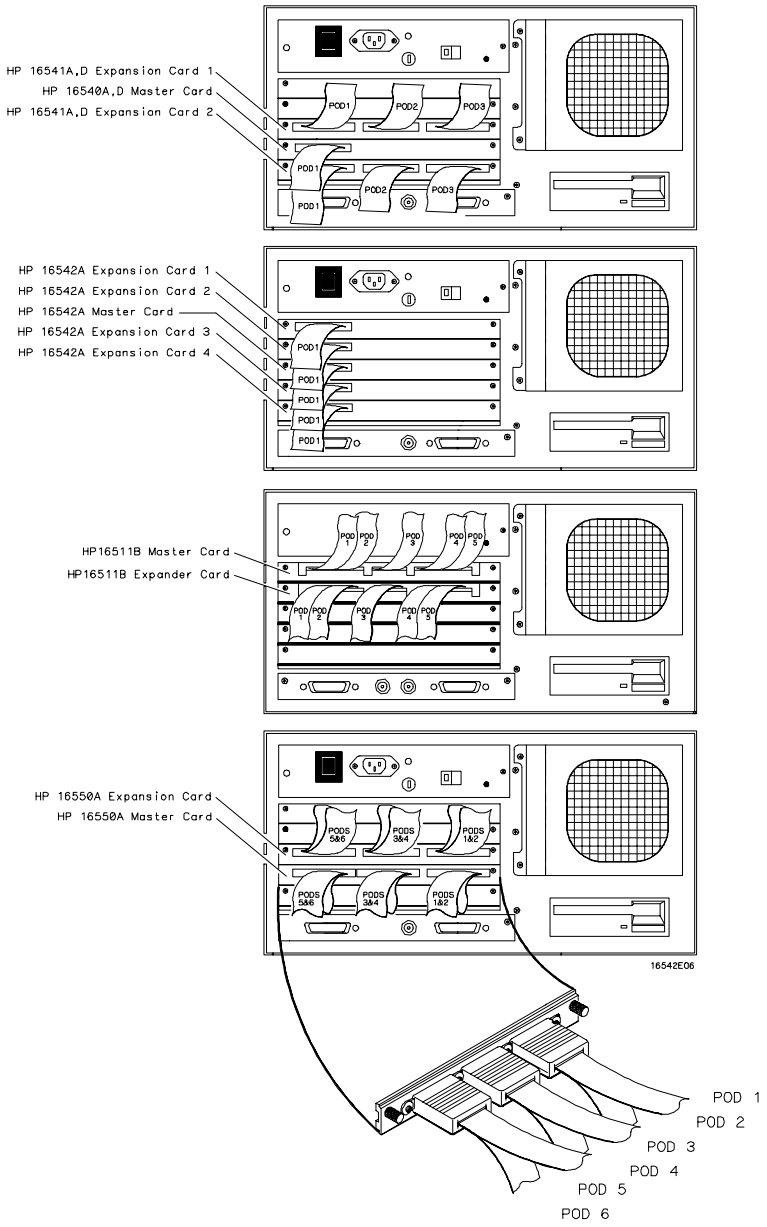

Figure 1-2. Logic Analyzer Card Locations
(relative locations, actual slots used may vary)

Setting Up the Analyzer from the Disk

The logic analyzer can be configured for 80386DX/DXL analysis by loading the appropriate configuration file. Loading this file will also load an inverse assembler file (IA386 or IA386E). To load the configuration file and inverse assembler:

1. Install the flexible disk in the front disk drive of the logic analyzer. (The HP 16500B mainframe has a hard disk drive. You can create a directory on the hard drive and copy the files from the flexible disk into the directory. For step two, select "Hard Disk.")
2. Select one of the following menus:
   - For the HP 1650-series logic analyzers, select the I/O Disk Operations menu;
   - For the HP 16500-series and HP 1660-series logic analyzers, select the System Front Disk menu.
3. Configure the menu to "Load" the analyzer configuration from disk.
4. For HP 16500-series and HP 1660-series logic analyzers, select the appropriate module (such as "100/500 MHz LA" or "Analyzer") for the load.
5. Use the knob to select the appropriate configuration file (see table 1-1).
6. Execute the load operation to load the file into the logic analyzer.

The IA386 inverse assembler works with the HP 1650A, HP 1650B, and HP 1652B Logic Analyzers, with the HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D, HP 16542A, and HP 16550A Logic Analyzers in an HP 16500A mainframe, and with the HP 1660A/61A Logic Analyzers with software versions V01.xx.

The IA386E inverse assembler contains enhanced features which use the increased capabilities of some of the logic analyzers. It works with the HP 16540/16541A,D and HP 16550A Logic Analyzers in an HP 16500B mainframe, and with the HP 1660A/61A Logic Analyzers with software version V02.00 or higher.

The configuration software checks the logic analyzer system configuration during the load process and automatically loads the appropriate inverse assembler.

2

Analyzing the Intel 80386DX/DXL

Introduction

This chapter provides reference information on the format specification and symbols configured by the HP E2444A software. It also contains information about the inverse assemblers, status encoding and timing analysis.

Format Specification

The 80386DX/DXL configuration files contain predefined format specifications. These format specifications include all labels for monitoring the 80386DX/DXL microprocessor and any coprocessors connected directly to the microprocessor (see figures 2-1, 2-2 and 2-3, which show the HP 16550A format specification). There are some slight differences in the displays, according to which logic analyzer you are using. For example, some logic analyzers do not have a Clock Period field. Refer to your logic analyzer manual to see which fields and displays are available.

Table 3-1 in chapter 3 lists the 80386DX/DXL signals for the HP E2444A Preprocessor Interface and their corresponding lines to the logic analyzers.

Note

For those logic analyzers which have a Clock Period field (HP 1650A, HP 1650B, HP 1652B, HP 16510A, HP 16510B, and HP 16511B), the Clock Period field should remain in the current selection (> 60 ns) for proper HP E2444A operation. For more information on the Clock Period field, refer to the reference manual for your logic analyzer.

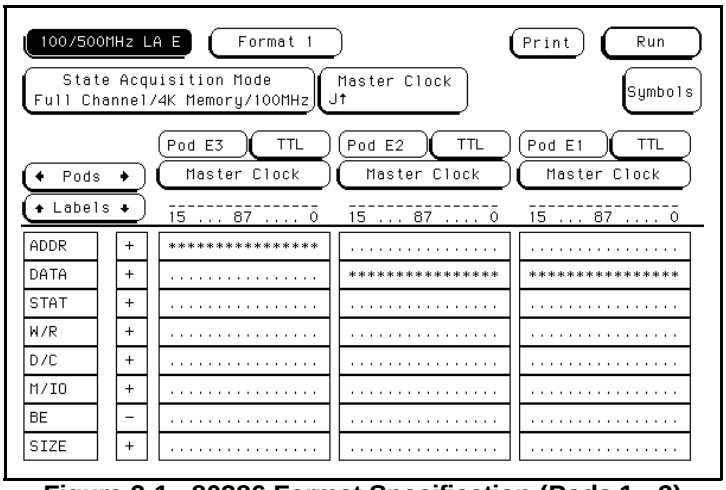

Figure 2-1. 80386 Format Specification (Pods 1 - 3)

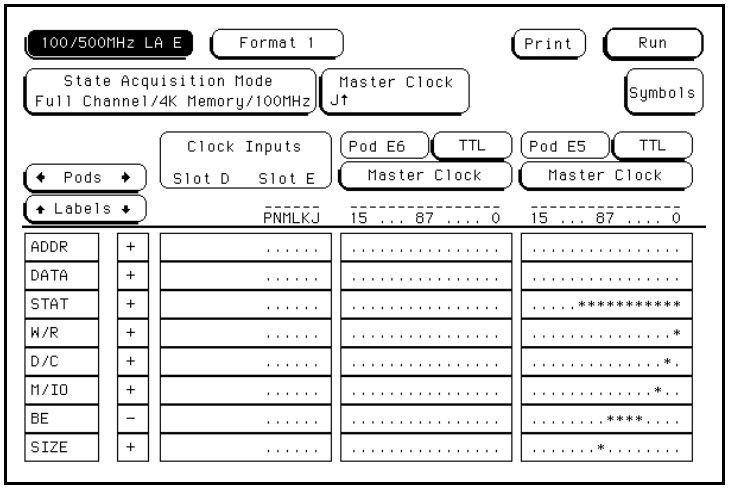

Figure 2-2. 80386 Format Specification (Pods 5 and 6)

Note

Additional labels are listed off the screen. To view these signals, select the Label field and rotate the knob on the front panel clockwise. Figure 2-3 shows some of the lower labels.

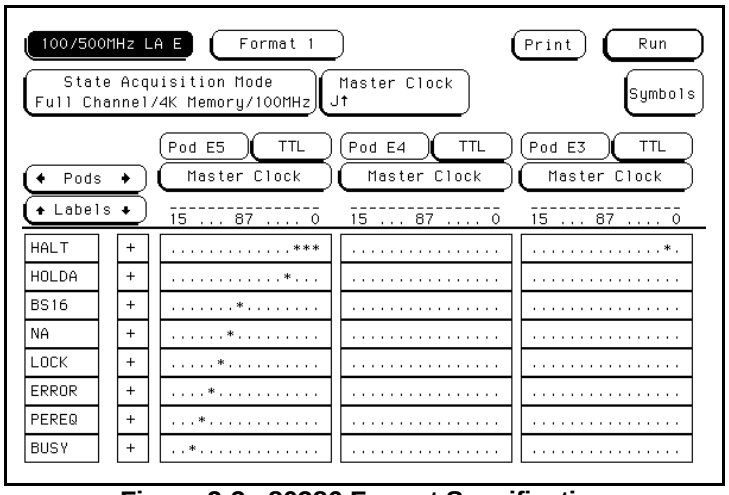

Figure 2-3. 80386 Format Specification (Pods 3 - 5, lower portion of display)

Symbols

The HP E2444A configuration software sets up symbol tables on the logic analyzers. The tables contain alphanumeric symbols which identify data patterns or ranges. Additional labels have been defined in the format specification menu to make triggering on specific 80386DX/DXL cycles easier. Four of the defined labels are:

- The "STAT" label, which displays 11 status lines.
- The "BE" label, which monitors BE0# to BE3# . These lines indicate valid bytes of the 32-bit data bus during specific transfers.
- The "SIZE" label, which indicates the size of the transfer on the data bus (16-bit or 32-bit transfer).
- The "HALT" label, which differentiates between a HALT cycle caused by executing the HALT instruction and a shutdown caused by protection fault while attempting to process a double fault.

Figures 2-4 and 2-5 show the symbol tables for the STAT and BE labels. Table 2-1 lists the bits assigned to the STAT label. Table 2-2 lists the Status Label encoding for all types of 80386DX/DXL microprocessor cycles.

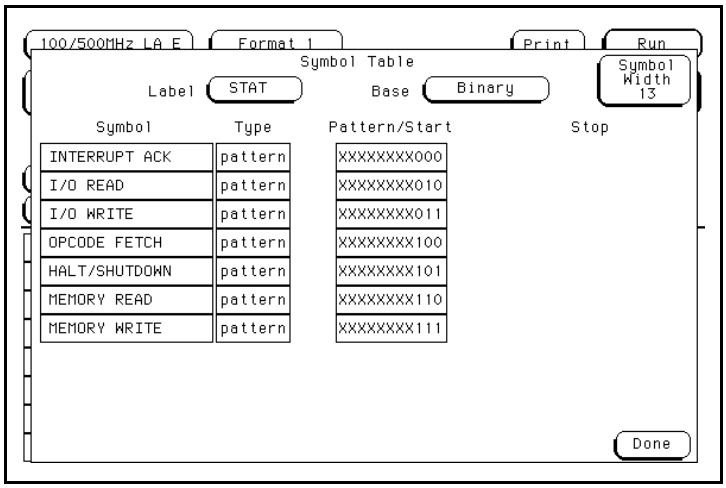

Figure 2-4. Symbol Table for the STAT Label

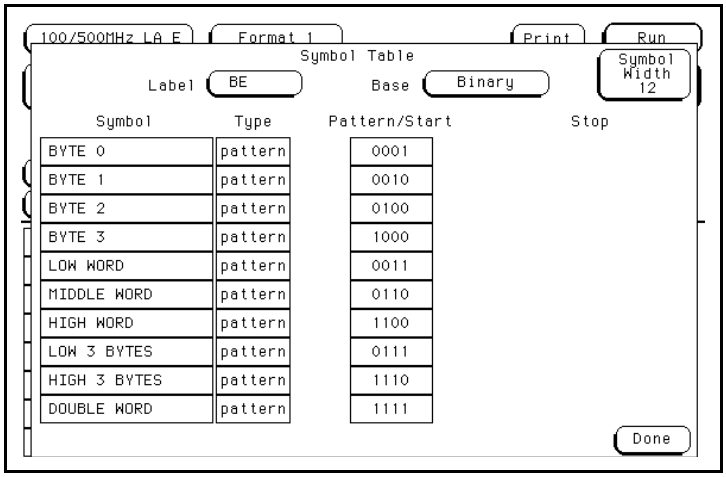

Figure 2-5. Symbol Table for the BE Label

Table 2-1. Description of the Status Bits

Bit	Status Signals	Description
0	D/C#	Signal is high for a data cycle and low for a control cycle.
1	M/IO#	Signal is high for memory and low for I/O.
2	W/R#	Signal is high for a write cycle and low for a read.
3	HLDA	Signal goes high when the microprocessor has relinquished control of the bus.

Table 2-1. Description of the Status Bits (Continued)

Bit	Status Signals	Description
4 - 7	BE0# - BE3#	Byte Enables, with BE0# the least significant byte and BE3# the most significant byte. For opcode fetches, the microprocessor will fetch four bytes unless BS16# is asserted. When BS16# is asserted, the microprocessor fetches two bytes.
8	BS16#	If this signal is low for a 16-bit bus cycle, the microprocessor will perform an additional bus cycle if required. For instance, if BS16# was low during a memory write with all byte enable (BE#) lines low, the microprocessor would perform a second bus cycle using the data from the upper two bytes of the data bus of the first cycle, on the lower two bytes of the data bus for the second cycle.
9	NA# *	When this signal is low it indicates that the system is requesting the next address from the microprocessor.
10	LOCK#	When this signal is low it indicates that the microprocessor has the bus locked to prevent interruption by other bus devices.
11	ERROR# *	When this signal is low it indicates that the previous coprocessor instruction generated a coprocessor error.
12	PEREQ *	When this signal is high it requests that the microprocessor perform a data operand transfer for a coprocessor extension.
13	BUSY# *	When this signal is low it indicates the coprocessor is still executing an instruction.
14	ADS# *	When this signal is low it indicates a valid bus cycle and address is available on the microprocessor pins.
15	READY# *	When this signal is low it terminates the bus cycle. This signal is ignored during bus hold acknowledge.

* These signals are used for timing analysis purposes when the HP E2444A is operating in the timing mode.

Table 2-2. Status Field Encoding

80386	Status Bit 10 9 8 7 6 5 4 3 2 1 0
Cycle Type	
Interrupt Acknowledge	x x x x x x x x 0 0 0
I/O Read	x x x x x x x x 0 1 0
I/O Write	x x x x x x x x 0 1 1
Opcode Fetch	x x x x x x x x 1 0 0
Halt/Shutdown	x x x x x x x x 1 0 1
Memory Read	x x x x x x x x 1 1 0
Memory Write	x x x x x x x x 1 1 1
Valid Bytes in Transfer (from BE0# through BE3#)	
Double Word (all bytes valid)	x x x 0 0 0 0 x x x x
Higher 3 Bytes	x x x 0 0 0 1 x x x x
High Word	x x x 0 0 1 1 x x x x
Byte 3	x x x 0 1 1 1 x x x x
Lower 3 Bytes	x x x 1 0 0 0 x x x x
Middle Word	x x x 1 0 0 1 x x x x
Byte 2	x x x 1 0 1 1 x x x x
Low Word	x x x 1 1 0 0 x x x x
Byte 1	x x x 1 1 0 1 x x x x
Byte 0	x x x 1 1 1 0 x x x x
Size of Transfer	
16-bit Transfer	x x 0 x x x x x x x x
32-bit Transfer	x x 1 x x x x x x x x

Note: X = don't care. The actual status field is a 15-bit field; however, bits 11 through 14 are not shown since they are "don't cares."

Listing Menu

Captured data is displayed in the Listing menu as shown in figure 2-6 (with the IA386 inverse assembler) or figure 2-7 (with the IA386E inverse assembler). The inverse assembler is constructed so the mnemonic output closely resembles the actual assembly source code.

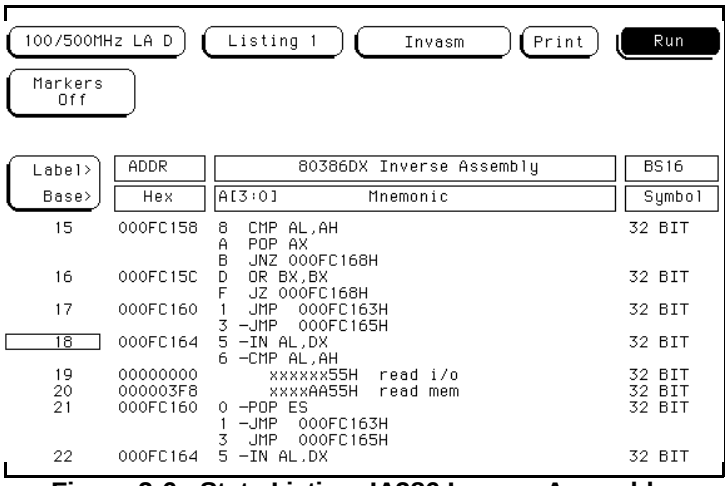

Figure 2-6. State Listing, IA386 Inverse Assembler

Note

If your state trace doesn't appear to be correct (capturing the same RAM address twice, for example), make sure the state/timing jumper J2 is open. If J2 is closed, remove the jumper and run the trace again.

Figure 2-7 shows the listing display with the IA386E inverse assembler (only available with some logic analyzers, see page 1-12). The unexecuted prefetches have been suppressed. A comparison of figures 2-6 and 2-7 shows the display filtering.

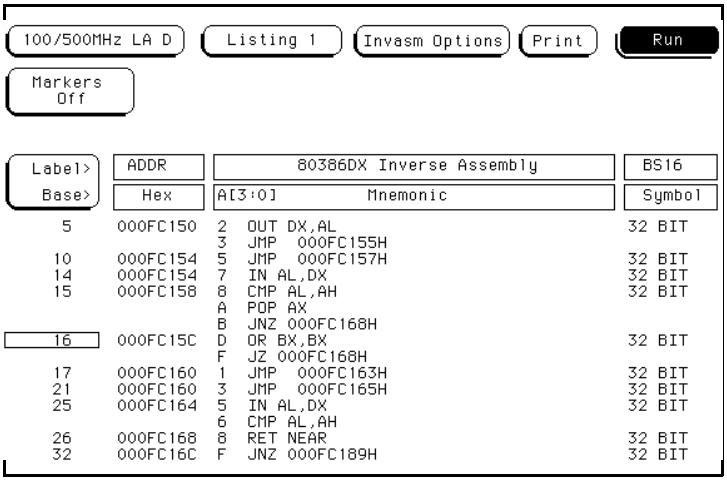

Figure 2-7. State Listing, IA386E Inverse Assembler (Unexecuted Prefetches Suppressed)

The 80386DX/DXL Inverse Assemblers

The 80386DX/DXL Preprocessor Interface software contains two inverse assemblers, IA386 and IA386E. IA386E contains additional features which use the increased capabilities of some of the logic analyzers (see page 1-12). For more information on the IA386E features, see "The IA386E Inverse Assembler".

The inverse assemblers have been designed to support the 80386DX/DXL microprocessor with or without coprocessors. The following paragraphs explain the operation of the inverse assemblers and the results you can expect in certain conditions.

The 80386DX/DXL microprocessor can fetch instructions up to 4 bytes (32 bits) wide in a single bus cycle. However, the microprocessor does not indicate externally which of the bytes fetched is the first byte of a code fetch. You must "point" to the first byte of an instruction fetch. Once synchronized, the inverse assemblers will disassemble from this state through the end of the screen.

In addition, the 80386DX/DXL microprocessor can execute two types of object code. The 80386DX/DXL can execute the 80386DX/DXL instruction set (32-bit), and it can also execute object code from Intel's 16-bit microprocessor family, including software designed for the Intel 8086 and the Intel 80286. The user must tell the logic analyzer what "size" of code is being executed by the microprocessor.

Note

Size, as used here, has no relationship to the physical size of the microprocessor's data bus. In this reference, size is used to indicate whether the code being executed was originally designed to run on Intel's 16-bit or 32-bit microprocessors.

Synchronizing the Inverse Assemblers

To point to the first byte of a code fetch and to indicate the size of the opcode, do the following:

1. Identify a line on the display that you know contains the first byte of an instruction fetch.
2. Roll this line to the top of the listing.

Note 

The cursor location is not the top of the listing. In figure 2-6, line 15 is the top of the listing.

---

3. For the IA386 inverse assembler, select the "Invasm" field at the top of the display. The pop-up shown in figure 2-8 will appear. For the IA386E inverse assembler, select the "Invasm Options" button and use the Code Synchronization portion of the submenu. The pop-up shown in figure 2-9 will appear.
4. Select the choice that identifies which byte of the captured state contains the first byte of the code fetch and what kind of object code is being executed by the microprocessor (Size 16 or 32 for Intel's 16- or 32-bit microprocessor families). With the IA386E inverse assembler, also select "Align".

The listing will inverse assemble from the top line down. Any data before this screen is left unchanged. Rolling the screen up will inverse assemble the lines as they appear on the bottom of the screen. If you jump to another area of the screen by entering a new line number, you must re-synchronize the inverse assembler by repeating the above steps.

Each time you inverse assemble a block of memory, the analyzer will keep that block in the inverse assembled condition. You can inverse assemble several different blocks in the analyzer memory, but the activity between those blocks will not be inverse assembled.

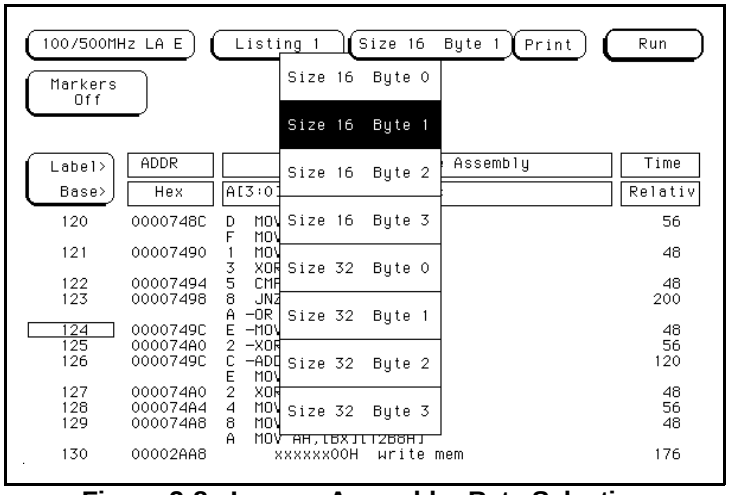

Figure 2-8. Inverse Assembler Byte Selection (IA386 Inverse Assembler)

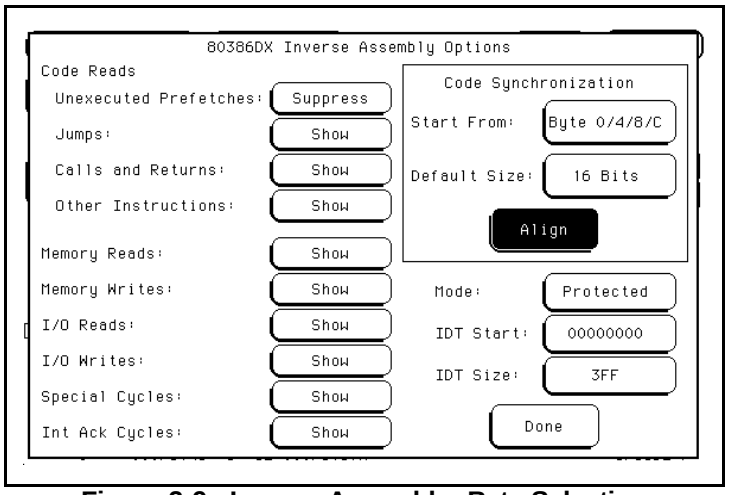

Figure 2-9. Inverse Assembler Byte Selection (IA386E Inverse Assembler)

Interpreting Data

Unless followed by a lower-case letter, all numeric output from the inverse assembler is in hexadecimal format. Decimal values are indicated by a lower-case "d" (as in the INT instruction).

Up to four instructions may be displayed for a single analyzer state, because the 80386DX/DXL can fetch a double word with four instruction bytes from program memory. If the least significant byte of this double word contains a single-byte instruction, the next sequential instruction begins in the next higher byte. This process continues from the least significant byte to the most significant byte until all of the bytes of the fetched double word are used. When a single state contains more than one instruction, each instruction will be displayed on a separate line. For example:

```
+ 0015    NEG ECX                          = OPCODE FETCH
          MOV BYTE PTR [EBP][-1B].CL       =
+ 0016    xxxxxxDA  READ MEM               = MEMORY READ
```

Line number + 0015 displays two instructions from a double-word.

Since instructions may begin in any byte position, the last bytes of a multiple-byte instruction may extend into the lower bytes of the next double word fetched. In this instance, the next sequential instruction begins in the next higher byte of the next double-word after the previous instruction and operands. When interpreting a given state, the inverse assembler will ignore bytes used by a previous instruction and will only display the instructions that begin in that state. For example:

Byte Position 3	2	1	0	
01	20	BB	24	Single byte instruction MOV BX (BB) starts in byte 1.
10	BF	D2	31	Double byte instruction XOR DX,DX (31D2) begins in byte 0 and continues into byte 1. Next instruction MOV DI (BF) begins in byte 2.
F7	C8	8C	00	Double byte instruction DIVDI (F7F7) starts in byte 3 and continues into byte 0 of next double word fetched.
30	CA	81	F7	Next instruction OR DX (81CA) begins in byte 2 immediately after last instruction.

Asterisks (*) in the inverse assembler output indicate that a portion (or portions) of an instruction was not captured by the analyzer. Missing opcodes occur frequently and are primarily due to microprocessor prefetch activity. Storage qualification, or the use of storage windows, can also lead to such occurrences.

The 80386DX/DXL has two possible default operand/address sizes, 16 or 32 bits. This attribute is set when a code segment descriptor is loaded, and is impossible for the inverse assembler to detect. Therefore, it must be declared manually by selecting the correct field under the "Invasm" pop-up. Any instruction with an operand size of 32 bits (either by default, or by using the operand override prefix) will be marked with an "= " symbol in the last column of the 80386DX/DXL mnemonic field to help you distinguish 32-bit operands from 16-bit operands.

If the inverse assembler seems to be disassembling incorrectly, and the problem is neither prefetch activity nor storage qualification, it is likely that the size attribute is set incorrectly.

The 80386DX/DXL microprocessor can perform byte, word, and three-byte transfers, as well as double-word transfers between microprocessor registers and memory. Byte transfers can occur in any byte on the 32-bit data bus. Word and three-byte transfers can occur across any contiguous set of bytes that will hold the transfer. The bytes that are valid in a transfer are indicated by the microprocessor BE0# through BE3# lines. The inverse assembler will display "xx" (don't care) for the bytes of a transfer that are ignored by the microprocessor. In this way it is possible to determine exactly which bytes were used by the microprocessor. For example:

xxxxxxDBH	read memory	(Byte transfer on byte 0)
xxxx28xxH	read memory	(Byte transfer on byte 1)
xxB3xxxxH	read memory	(Byte transfer on byte 2)
ECxxxxxxH	read memory	(Byte transfer on byte 3)
xxxx28DBH	read memory	(Word transfer on lower word)
xxB328xxH	read memory	(Word transfer on middle word)
ECB3xxxxH	read memory	(Word transfer on upper word)
xxB328DBH	read memory	(3-byte transfer on lower three bytes)
ECB328xxH	read memory	(3-byte transfer on upper three bytes)
ECB328DBH	read memory	(Double-word transfer)

Physical, rather than logical addresses, are used to perform symbolic address mapping. Most instructions, however, specify a 32-bit intrasegment offset and may indicate a segment different from the default segment for that particular instruction. Since the physical address cannot be determined from this information alone, the inverse assembler must attempt to locate the resulting bus cycle so that the physical address may be obtained. If a bus cycle of the type indicated by the initiating instruction is not found, the physical address cannot be determined and an unmapped logical address (segment override, if any, and the 32-bit intrasegment offset) is displayed instead of a mapped physical address.

Error Messages

Any of the following list of error messages may appear during analysis of your target software. Included with each message is a brief explanation.

Illegal Task Request	Displayed if the inverse assembler is used with an instrument other than the supported logic analyzers.
Fatal Data Error	Displayed if the trace memory could not be read properly on entry into the inverse assembler.
Invalid Status	Displayed if the status field for the current state is not valid.
Illegal Opcode	Displayed if the inverse assembler encounters an illegal 80386DX/DXL instruction.
Reserved Opcode	Displayed if the inverse assembler encounters a reserved coprocessor instruction.
No Operand	Displayed if the inverse assembler cannot find a complete operand field for an instruction. Prefetch activity or storage qualification is often the cause.

Instruction Decoding (-/?)

The HP E2444A Preprocessor Interface will send all of the bus transactions by both the microprocessor and coprocessor to the logic analyzer. The time count will accurately reflect when the end of the bus cycle occurred. Prefetched instructions which are not executed by the microprocessor are marked by a hyphen "-". Typically, several states separate the memory (or I/O) transfer from the instruction that caused the transfer.

The logic analyzer captures prefetches, even if they are not executed. Care must be taken when you are specifying a trigger condition or a storage qualification and the instruction of interest follows an instruction that may cause branching. An unused prefetch may generate an unwanted trigger.

Since the microprocessor only prefetches at most four words, one technique to avoid unwanted triggering from unused prefetches is to add "10 hex" to the trigger address. This trigger condition will only be satisfied if the branch is not taken.

In some cases, it is impossible to determine from bus activity whether or not a branch is taken or a prefetch is executed. In these cases, the inverse assembler marks the disassembled line with the prefix "?".

The logic analyzer is clocked once each bus cycle. The preprocessor interface hardware ensures that the logic analyzer will reliably capture the address, data, and status information during both pipelined and non-pipelined cycles by latching this information during the current bus cycle and sending it to the logic analyzer during the succeeding bus cycle. See the "Preprocessor Interface Description" section in Chapter 3 for complete details of this process.

Coprocessor Support

The HP E2444A Preprocessor Interface and Inverse Assembler fully supports the 80287 and 80387 math coprocessors instructions.

Additional Information on Instruction Decoding

A 32-bit memory cycle on a 16-bit bus is sent to the logic analyzer as two bus transactions (see figure 2-10).

The preprocessor interface stops generating logic analyzer clocks when the 80386DX/DXL asserts HLDA. Bus cycles that assert HLDA, such as DMA cycles, will not be captured by the logic analyzer.

Note

The ADS and READY lines must be operating in normal 80386DX/DXL bus cycles when the HLDA line is disabled. If these lines are not present during the HLDA (hold acknowledge) period, the preprocessor interface will not remain in step with following bus cycles. This will result in incorrect capturing of data.

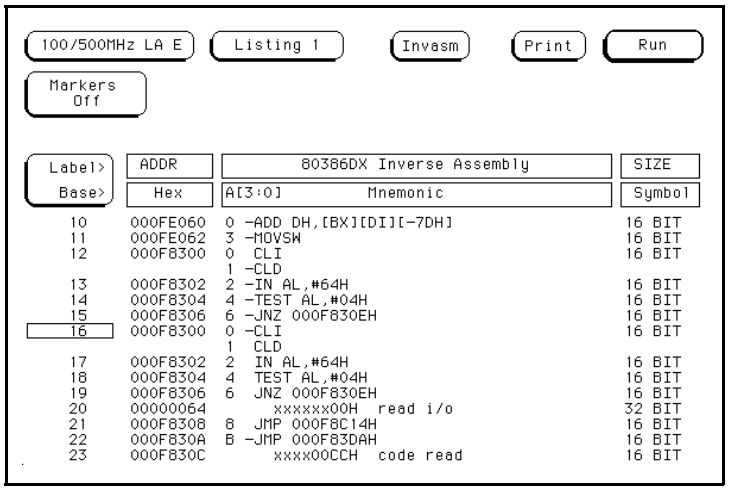

Figure 2-10. 80386 2-Byte Mode

The IA386E Inverse Assembler

The IA386E inverse assembler contains additional features which use the increased capabilities of some of the logic analyzers (see page 1-12 for supported logic analyzers). For those logic analyzer systems, the IA386E inverse assembler is automatically loaded when the appropriate configuration file is loaded. Note that all the features in the IA386 inverse assembler are also included in the IA386E inverse assembler (see previous sections).

The IA386E Inverse Assembly Options menu contains three functions: display filtering with Show/Suppress selections, Code Synchronization, and IDT description entry (see figure 2-11). The following sections describe these functions.

Note

If the X or O pattern markers are turned on, and the designated pattern is found in a state that has been Suppressed with display filtering, the following message will appear on the logic analyzer display: "X (or O) pattern found, but state is suppressed."

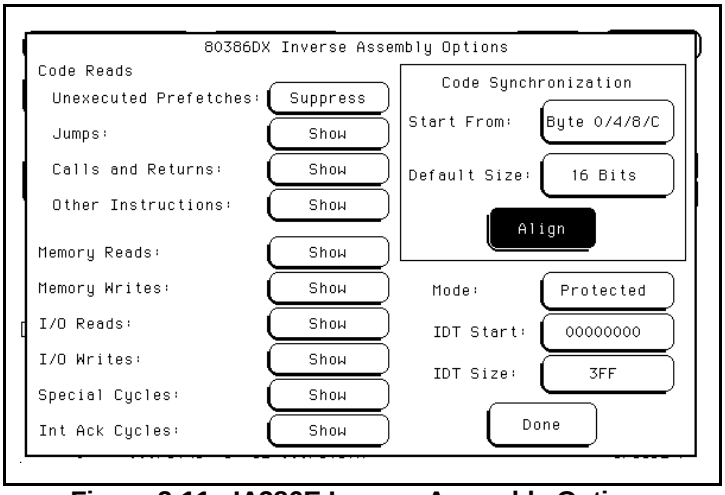

Figure 2-11. IA386E Inverse Assembly Options

Show/Suppress

The Suppress/Show settings determine whether the various microprocessor operations are shown or suppressed on the logic analyzer display. Figure 2-11 shows the microprocessor operations which have this option. The settings for the various operations do not affect the data which is stored by the logic analyzer, they only affect whether that data is displayed or not. The same data can be examined with different settings, for different analysis requirements.

This function allows faster analysis in two ways. First, unneeded information can be filtered out of the display. Figure 2-11 shows the settings to suppress unexecuted prefetches. Figure 2-7 (page 2-9) shows a listing with the unexecuted prefetches suppressed, so that only executed instructions are displayed. A comparison of figures 2-7 and 2-6 (page 2-8) shows the difference in the listing display.

Second, particular operations can be isolated by suppressing all other operations. For example, I/O accesses can be shown, with all other operations suppressed, allowing quick analysis of I/O accesses.

Code Synchronization

The Code Synchronization enables the inverse assembler to resynchronize with the microprocessor code. In some cases the prefetch marking algorithm in the inverse assembler may lose synchronization, and unused prefetches or executed instructions may be incorrectly marked. If any of the Code Reads are suppressed, this could cause some executed instructions to be missing from the display.

To resynchronize the inverse assembler, use the procedure on page 2-11.

IDT Description

The IDT Description settings include Mode, IDT Start, and IDT Size. Mode can be Protected, Real, or Virtual. IDT Start refers to the starting address of the Interrupt Descriptor Table, and IDT Size refers to the size of the table. Set these functions to match the target system settings.

In most cases, the inverse assembler can automatically determine the target system settings, and will operate properly regardless of the settings entered. The inverse assembler uses the information from these settings only in cases of uncertainty. If you suspect that the inverse assembler is disassembling improperly, check that these settings match your target system.

Timing Analysis

The same format specification loaded for state analysis is also used for timing analysis. To configure the logic analyzer for timing analysis:

1. Configure the HP E2444A for timing analysis by installing the jumper on J2 (see page 1-4).
2. Select the Configuration menu of the logic analyzer.
3. Select the Type field for the 80386DX/DXL analyzer and select Timing (see figure 2-12).

Note

BS16 and RESET are not available for timing analysis.

BS16 appears on the format specification, but is not accurate for timing analysis because it is delayed by an edge-triggered latch on the preprocessor interface board.

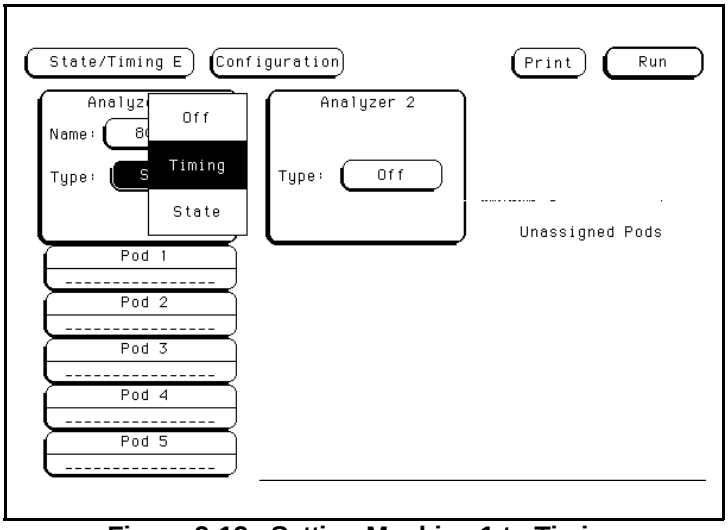

Figure 2-12. Setting Machine 1 to Timing

Timing Format Specification

When the preprocessor interface is used for timing analysis, the format specification will be set up as shown in figures 2-13 and 2-14. Additional labels which are listed off screen. To view these signals, select the Label field and rotate the knob on the front panel clockwise.

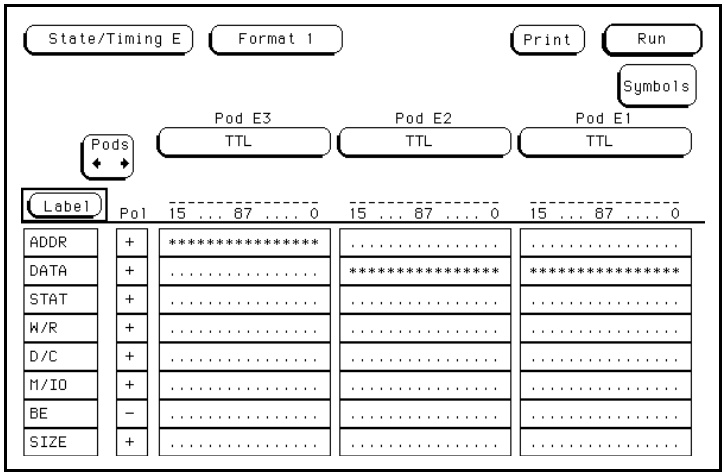

Figure 2-13. Timing Format Specification (Pods 1-3)

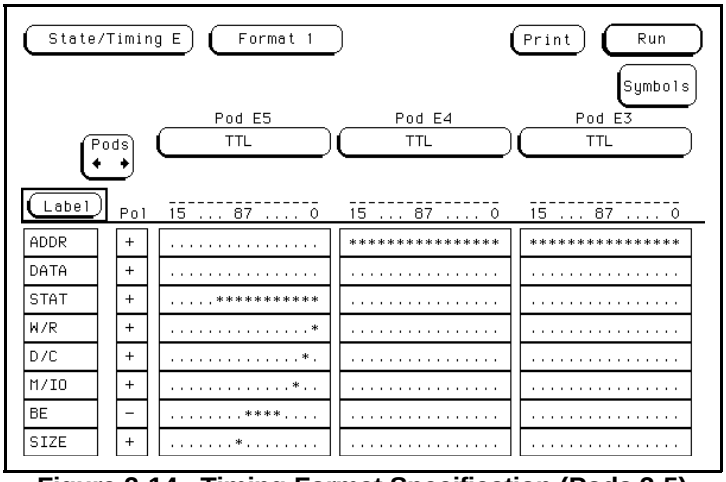

Figure 2-14. Timing Format Specification (Pods 3-5)

Waveform Menu

Captured data is displayed in the Waveform menu as shown below.

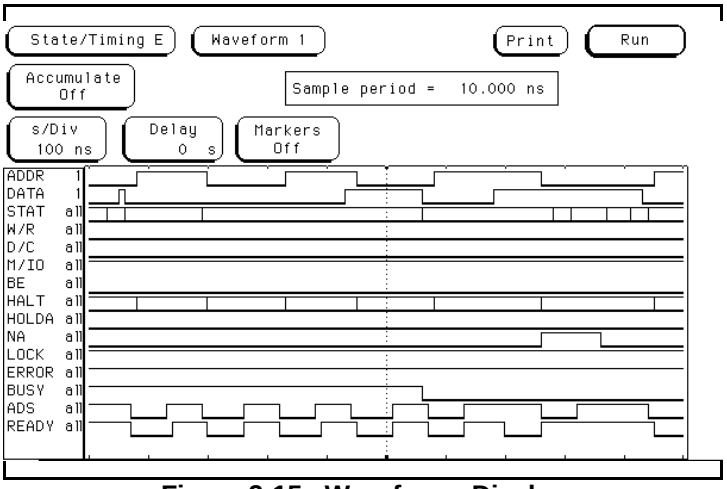

Figure 2-15. Waveforms Display

State-Per-Clock Mode

State-Per-Clock mode clocks the logic analyzer on every K clock rising and falling edge regardless of whether or not valid transfers occur; therefore, every state which crosses the target system microprocessor's bus is captured. This allows the logic analyzer to capture wait states and idle states, in addition to valid address states and data states.

To select State-Per-Clock mode, install the jumper on J2, and change the Clock field to K⇕. Note that inverse assembly is not supported in State-Per-Clock mode.

3

General Information

Preprocessor Interface Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the HP E2444A Preprocessor Interface. These characteristics are included as additional information for the user.

Microprocessor Compatibility: Intel 80386DX/DXL and all microprocessors made by other manufacturers that comply with Intel 80386DX/DXL specifications. The HP E2444A also supports static microprocessors such as the Am 386DXL.

CPU Package Supported: 132-pin PGA

Maximum Clock Speed: 40 MHz clock output (CLK); 80 MHz clock input (CLK2).

State Speed: Four CLK2 cycles per bus cycle.

Maximum Analyzer Clock Speed: 20 MHz state speed with CLK2 at 80 MHz.

Signal Line Loading: Approximately 15 pF on ADS and READY.

Approximately 8 pF on all other lines.

Microprocessor Operations Displayed:
Memory Read/Write
I/O Read/Write
Opcode Fetch
Interrupt Acknowledge Type 0-255
Halt
Shutdown
80287 or 80387 Coprocessor Operations

Timing Analysis: All signals are buffered by a 74FCT646ATQ gate, with a 2 ns channel-to-channel skew.

Power Requirements: 1.0 A at + 5 Vdc maximum, supplied by the logic analyzer.

Logic Analyzer Required:	HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D (Master Card and two expansion cards), HP 16542A (Master Card and four expansion cards), or HP 16550A	
Number of Probes Used:	Five 16-channel probes	
Environmental Temperature:	Operating:	0 to + 55 degrees C (+ 32 to + 131 degrees F)
	Nonoperating:	-40 to + 75 degrees C (-40 to + 167 degrees F)
Altitude:	Operating:	4600 m (15,000 ft)
	Nonoperating:	15,300 m (50,000 ft)
Humidity:	Up to 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.	

Preprocessor Interface Description

The primary function of the HP E2444A Preprocessor Interface is to connect the target microprocessor to the logic analyzer, and to perform the interface logic required to identify address pipelining and 16-bit or 32-bit cycles. The HP E2444A Preprocessor Interface performs this primary function by:

- Latching and buffering the address, status, and data bus of the 80386DX/DXL microprocessor so that address, status, and data can be sent to the logic analyzer at the same time.
- Generating the logic analyzer clock from the appropriate 80386DX/DXL microprocessor signals and bus conditions.
- Synthesizing address lines A0 and A1 from the BE0# through BE3# lines so that the inverse assembler can identify the address for A0 and A1.

The preprocessor interface duplicates the internal CLK signal of the 80386DX/DXL by dividing the CLK2 signal by 2 and selecting the correct phase of the resulting signal. This signal is called CLK and is used to identify 80386DX/DXL activities inside the HP E2444A PAL.

The preprocessor interface detects the start of an 80386DX/DXL bus cycle when ADS# goes true. The preprocessor interface latches address and status on the following conditions:

- If the 80386DX/DXL cycle is a non-pipelined cycle, address and status are latched during the time that ADS# is low.
- If the 80386DX/DXL cycle is a pipelined cycle, address and status are latched during the first CLK2 cycle after READY# is detected low.

Data is latched at the end of the 80386DX/DXL cycle. The end of the bus cycle is defined as the rising edge of CLK2 when CLK is high and READY# is low. The clock for the logic analyzer is generated approximately 8 ns after the end of the cycle. The J clock for latching information into the logic analyzer is generated by the PAL on the HP E2444A each time the READY# signal goes low.

The K clock is for State-Per-Clock mode. It is one half the frequency of the 80386 CLK2; however, it clocks the logic analyzer on both the rising and the falling edges.

Figure 3-1 shows a block diagram of the HP E2444A Preprocessor Interface. The timing diagram (figure 3-2) shows the time at which address and data are sampled.

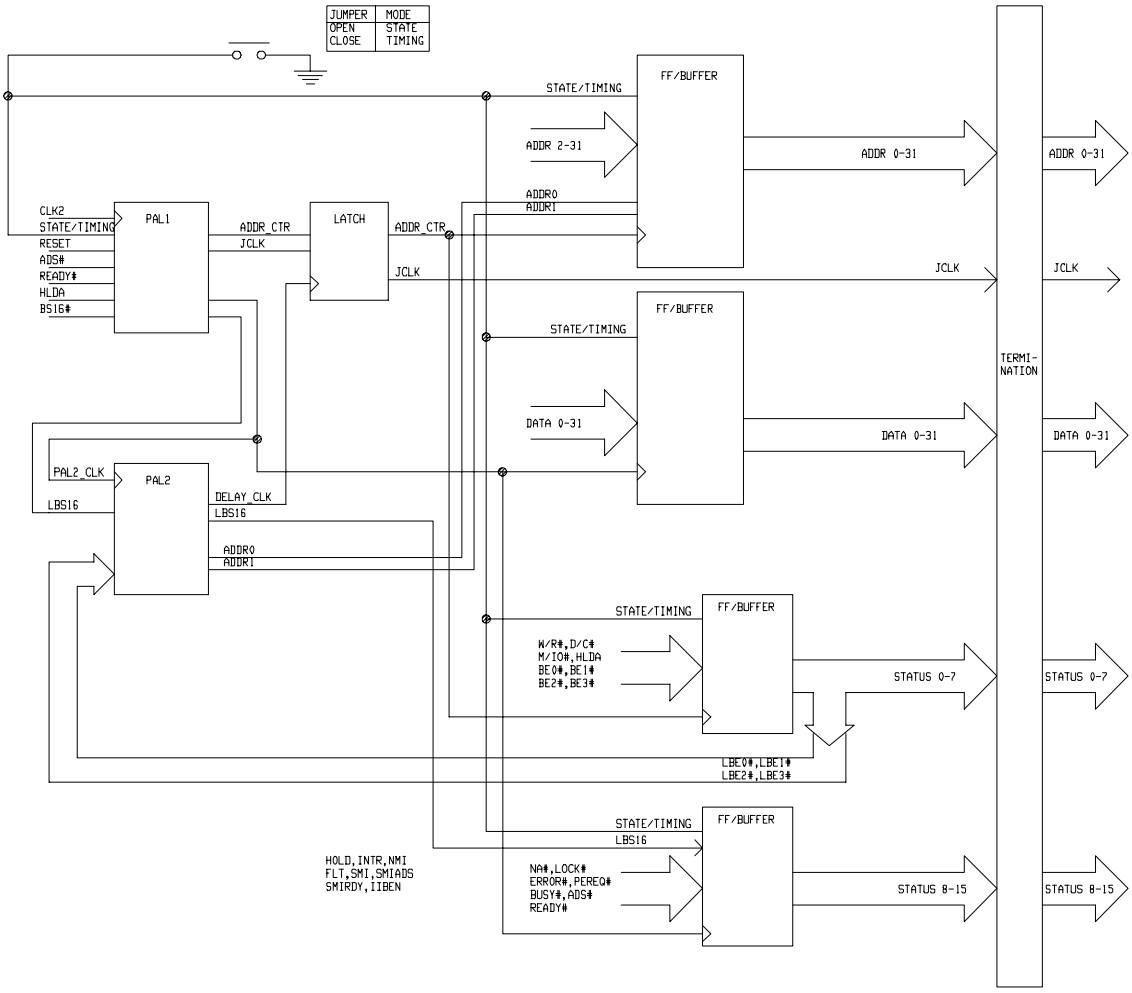

Figure 3-1. HP E2444A Block Diagram

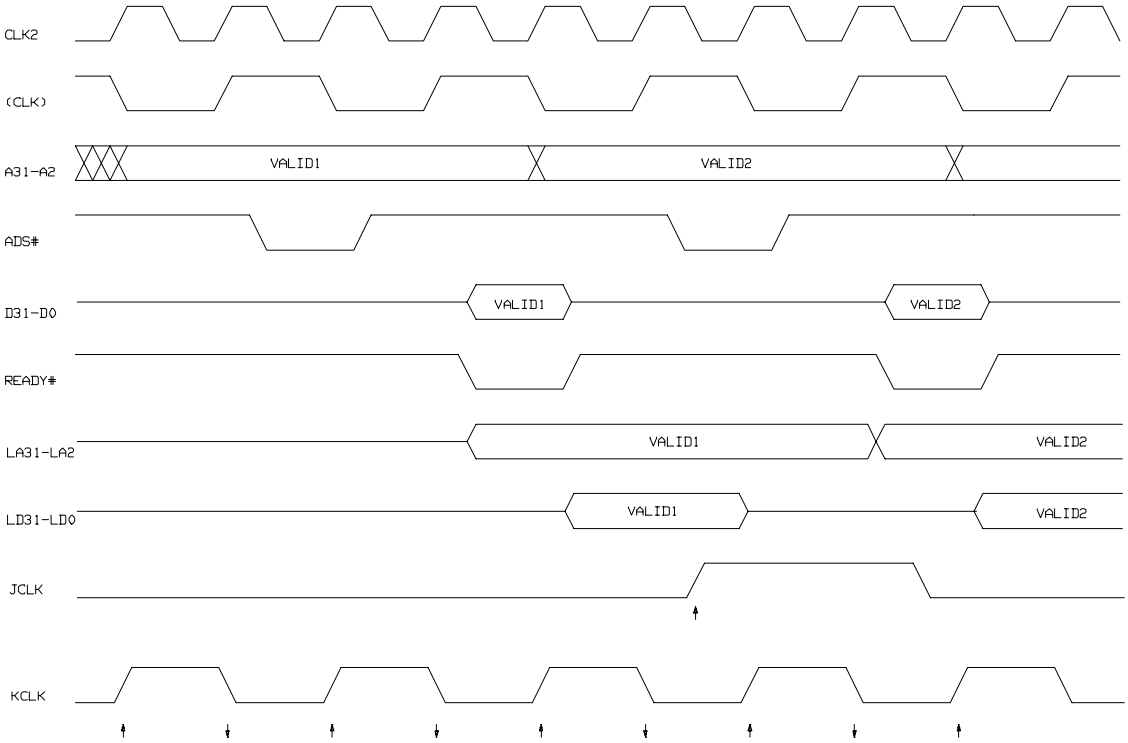

Figure 3-2. HP E2444A Timing Diagram

80386DX/DXL Signal to HP E2444A Connector Mapping

The following table describes the electrical interconnections implemented with the HP E2444A Preprocessor Interface. Since the pods on the logic analyzers may be numbered differently than the pods on the preprocessor interface, refer to table 1-1 to correlate the pod numbers.

Note

The interconnections implemented with the HP E2444A are not direct interconnections. The HP E2444A Preprocessor Interface places digital circuitry between the microprocessor pin and the logic analyzer input.

Table 3-1. 80386DX/DXL Signal List

Preprocessor Pod	Logic Analyzer Probe	80386DX/DXL Pin Number	Pin Mnemonic	Label
P5	0	B10	W/R#	STAT
P5	1	A11	D/C#	STAT
P5	2	A12	M/IO#	STAT
P5	3	M14	HLDA	STAT
P5	4	E12	BE0#	STAT
P5	5	C13	BE1#	STAT
P5	6	B13	BE2#	STAT
P5	7	A13	BE3#	STAT
P5	8	C14	BS16#	STAT
P5	9	D13	NA#	STAT
P5	10	C10	LOCK#	STAT
P5	11	A8	ERROR#	STAT
P5	12	C8	PEREQ	STAT
P5	13	B9	BUSY#	STAT
P5	14	E14	ADS#	STAT
P5	15	G13	READY#	STAT

Table 3-1. 80386DX/DXL Signal List (continued)

Preprocessor Pod	Logic Analyzer Probe	80386DX/DXL Pin Number	Pin Mnemonic	Label
P3	0	*	A0	ADDR
P3	1	*	A1	ADDR
P3	2	C4	A2	ADDR
P3	3	A3	A3	ADDR
P3	4	B3	A4	ADDR
P3	5	B2	A5	ADDR
P3	6	C3	A6	ADDR
P3	7	C2	A7	ADDR
P3	8	C1	A8	ADDR
P3	9	D3	A9	ADDR
P3	10	D2	A10	ADDR
P3	11	D1	A11	ADDR
P3	12	E3	A12	ADDR
P3	13	E2	A13	ADDR
P3	14	E1	A14	ADDR
P3	15	F1	A15	ADDR
P4	0	G1	A16	ADDR
P4	1	H1	A17	ADDR
P4	2	H2	A18	ADDR
P4	3	H3	A19	ADDR
P4	4	J1	A20	ADDR
P4	5	K1	A21	ADDR
P4	6	K2	A22	ADDR
P4	7	L1	A23	ADDR

* Derived from BE0# through BE3# .

Table 3-1. 80386DX/DXL Signal List (continued)

Preprocessor Pod	Logic Analyzer Probe	80386DX/DXL Pin Number	Pin Mnemonic	Label
P4	8	L2	A24	ADDR
P4	9	K3	A25	ADDR
P4	10	M1	A26	ADDR
P4	11	N1	A27	ADDR
P4	12	L3	A28	ADDR
P4	13	M2	A29	ADDR
P4	14	P1	A30	ADDR
P4	15	N2	A31	ADDR
P1	0	H12	D0	DATA
P1	1	H13	D1	DATA
P1	2	H14	D2	DATA
P1	3	J14	D3	DATA
P1	4	K14	D4	DATA
P1	5	K13	D5	DATA
P1	6	L14	D6	DATA
P1	7	K12	D7	DATA
P1	8	L13	D8	DATA
P1	9	N14	D9	DATA
P1	10	M12	D10	DATA
P1	11	N13	D11	DATA
P1	12	N12	D12	DATA
P1	13	P13	D13	DATA
P1	14	P12	D14	DATA
P1	15	M11	D15	DATA
P1	J CLK			

Table 3-1. 80386DX/DXL Signal List (continued)

Preprocessor Pod	Logic Analyzer Probe	80386DX/DXL Pin Number	Pin Mnemonic	Label
P2	0	N11	D16	DATA
P2	1	N10	D17	DATA
P2	2	P11	D18	DATA
P2	3	P10	D19	DATA
P2	4	M9	D20	DATA
P2	5	N9	D21	DATA
P2	6	P9	D22	DATA
P2	7	N8	D23	DATA
P2	8	P7	D24	DATA
P2	9	N6	D25	DATA
P2	10	P5	D26	DATA
P2	11	N5	D27	DATA
P2	12	M6	D28	DATA
P2	13	P4	D29	DATA
P2	14	P3	D30	DATA
P2	15	M5	D31	DATA
P2	K CLK			

Servicing

The repair strategy for the HP E2444A is board replacement. However, table 3-2 lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Hewlett-Packard Sales/Service Office for further information on servicing the board.

Exchange assemblies are available when a repairable assembly is returned to Hewlett-Packard. These assemblies have been set up on the "Exchange Assembly" program. This allows you to exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

Table 3-2. Replaceable Parts

HP Part Number	Description
E2444-69501	Exchange Board/Cable Assembly
E2444-68702	Software Disk Pouch
1200-1605 *	Pin Protector
1252-3743	Jumper

* The Pin Protector IC socket is also available from McKenzie Technology, part number PGA-132H004B1-1414R.

Dimensions

Figure 3-3 lists the dimensions for the HP E2444A circuit board. The dimensions are listed in inches and millimeters.

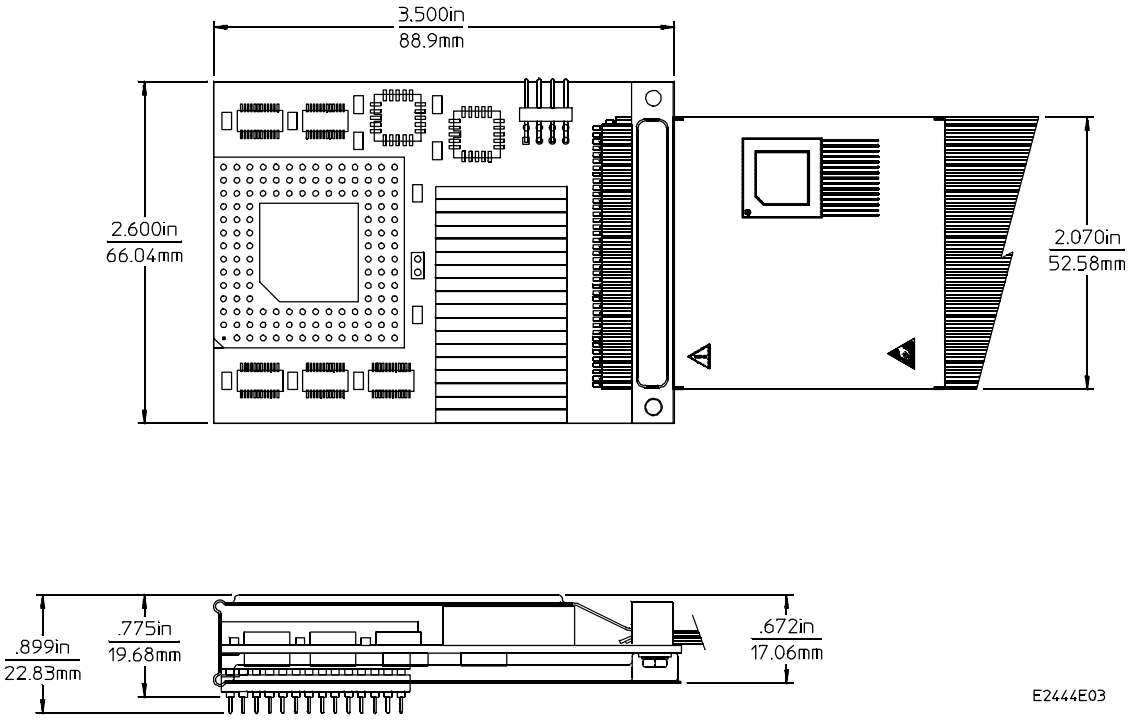

Figure 3-3. HP E2444A Dimensions - inches (mm)

A

Troubleshooting

If you encounter difficulties while making measurements, use this section to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions. Error messages which may appear on the logic analyzer are listed below in quotes " ". Symptoms are listed without quotes.

If you are still having difficulties after trying the suggestions below, please contact your local Hewlett-Packard service center for additional assistance.

Target Board Will Not Bootup

If the target board will not bootup after connecting the preprocessor interface, the microprocessor or the preprocessor interface may not be installed properly, or they may not be making electrical contact.

- Verify that the microprocessor and the preprocessor interface are properly rotated and aligned.
- Verify that the microprocessor and the preprocessor interface are securely inserted into their respective sockets.
- Verify that the logic analyzer cables are in the proper sockets of the preprocessor interface and firmly inserted.
- Reduce the number of extender sockets (see also "Capacitive Loading").

"Slow or Missing Clock"

This error message might occur if the logic analyzer cards are not firmly seated in the HP 16500A/B or HP 16501A frame. Ensure that the cards are firmly seated.

This error might also occur if the target system is not running properly. Ensure that the target system is on and operating properly.

If the error message persists, check the that the logic analyzer pods are connected to the proper connectors, as listed in table 1-1.

For HP 1650A and HP 16510A Logic Analyzers, check the preprocessor interface power fuse in the logic analyzer.

Slow Clock

If you have the preprocessor interface hooked up and running and observe a slow clock or no activity from the interface board, the + 5 V supply coming from the analyzer may not be getting to the interface board.

To check the + 5 V supply coming from the analyzer, disconnect one of the logic analyzer cables from the HP E2444A and measure across pins 1 and 2 or pins 39 and 40 (see figure A-1).

- If + 5 V isn't observed across these pins, check the internal preprocessor fuse or current limiting circuit on the logic analyzer. For information on checking this fuse or circuit, refer to the service manual for your logic analyzer.
- If + 5 V is observed across these pins and you feel confident that the + 5 V is getting to the preprocessor interface, contact your nearest Hewlett-Packard Sales/Service Office for information on servicing the board.

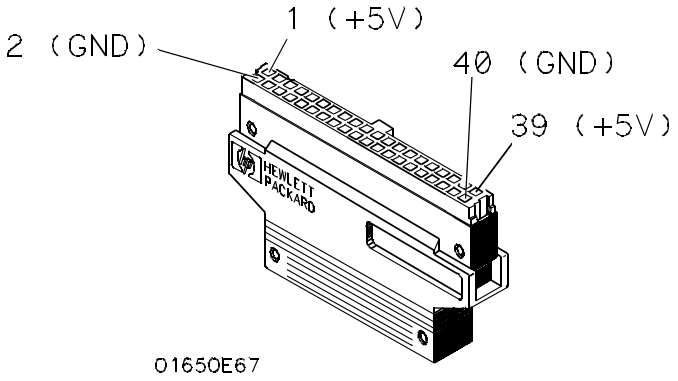

Figure A-1. Pinout of the Logic Analyzer Cable

"No Configuration File Loaded"

Verify that the appropriate module has been selected from the Load {module} from File {filename} in the HP 16500A/B disk operation menu. Selecting Load {All} will cause incorrect operation when loading most preprocessor interface configuration files.

"Selected File is Incompatible"

The logic analyzer displays this message if you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted.

No Inverse Assembly

Verify that the inverse assembler has been synchronized by placing an opcode at the top of the display (not at the input cursor) and pressing the Invasm key (see "Inverse Assembler" in Chapter 2).

Incorrect Inverse Assembly

This problem is usually caused by a hardware problem in the target system. A locked status line will often cause incorrect or incomplete inverse assembly.

- Check the activity indicators for status lines locked in a high or low state.
- Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values. These labels must remain as they are configured by the configuration file.
- Verify that the memory manager has been disabled. In most cases, if the microprocessor memory manager remains enabled you should still get inverse assembly, but it may be incorrect since some of the execution trace was not visible to the logic analyzer.
- Verify that storage qualification has not excluded storage of all the needed opcodes and operands.

No Activity on Activity Indicators

On the HP 1650A, HP 1651A, and HP 16510A Logic Analyzers if there is no activity the fuse which allows power to the preprocessor interface is probably blown. Check the fuse in the logic analyzer. On the other logic analyzers, if there is no activity, one of the cables, board connections, or preprocessor interface connections is probably loose. Check all connections.

Capacitive Loading

Excessive capacitive loading can cause signals to degrade, resulting in incorrect capture by the preprocessor interface or system lockup in the microprocessor. All preprocessor interfaces add additional capacitive loading. The following techniques will reduce the capacitive loading:

- Remove as many pin protectors, extenders, and adapters as possible.
- If multiple preprocessor interface solutions are available, try using one with lower capacitive loading.

"State Clock Violates Overdrive Specification"

At least one 16-channel pod in the state analysis measurement stored a different number of states before trigger than the other pods. This is usually caused by sending a clocking signal to the state analyzer that does not meet all of the specified conditions, such as minimum period, minimum pulse width, or minimum amplitude. Poor pulse shaping could also cause this problem.

Note 

The error message "State Clock Violates Overdrive Specification" should only occur for HP 1650A,B, HP 1652B, HP 16510A,B, and HP 16511B Logic Analyzers with the Clock Period field set to < 60 ns. If this error message is observed with the Clock Period set to > 60 ns, you may have a faulty logic analyzer. If a failure is suspected in your logic analyzer, contact your nearest Hewlett-Packard Sales/Service Office for information on servicing the instrument.

Unwanted Triggers

Unwanted triggers can be caused by unexecuted prefetches. Add the prefetch queue depth to the trigger address to avoid this problem.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern did not occur. Verify that the triggering pattern is correctly set.

If a "don't care" trigger condition is set, this message indicates:

- For an HP 16511B Logic Analyzer, only one of the two cards is receiving its state clock.
- For an HP 1650A,B, HP 1652B, or HP 16510A,B Logic Analyzer, the pattern duration is probably set to less than (<) instead of greater than (>). Since a "don't care" pattern is always true, the "less than" condition is never satisfied. Set the trace menu correctly for the measurement that is desired.

Intermittent Data Errors

This problem is usually caused by incorrect signal levels. Adjust the threshold level of the data pod. Use an oscilloscope to check the signal integrity of the data lines, as needed.

Bent Pins

Bent pins on the preprocessor interface, pin protectors, or adapters can cause system errors or inverse assembly errors. Ensure all pins are properly aligned and making contact.

"Time from Arm Greater Than 41.93 ms."

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

No Setup/Hold Field on Format Screen

The HP 16540/16541A,D or HP 16542A Logic Analyzer cards are not calibrated. Refer to your logic analyzer reference manual for procedures to calibrate the cards.

"Default Calibration Factors Loaded" (16540/41/42)

The default calibration file for the logic analyzer was loaded. The logic analyzer must be calibrated when using HP 16540A,D, HP 16541A,D or HP 16542A cards. Refer to your logic analyzer manual for procedures to calibrate the master clocking system, and ensure that the "cal factors" file is saved.

Herstellerbescheinigung

Hiermit wird bescheinigt, daB das Gerät/System

HP 1650A/B and HP 1651A/B

in Übereinstimmung mit den Bestimmungen von Postverfügung 1046/84 funkentstört ist.

Der Deutschen Bundespost wurde das Inverkehrbringen dieses Gerätes/Systems angezeigt und die Berechtigung zur Überprüfung der Serie auf Einhaltung der Bestimmungen eingeräumt.

Zusatzinformation für MeB- und Testgeräte

Werden MeB- und Testgeräte mit ungeschirmten Kabeln und/oder in offenen MeBaufbauten verwendet, so ist vom Betreiber sicherzustellen, daB die Funk-Entstörbestimmungen unter Betriebsbedingungen an seiner Grundstücksgrenze eingehalten werden.

Manufacturer's declaration

This is to certify that this product HP 1650A/B andd HP 1651A/B meets the radio frequency interference requirements of directive 1046/84. The German Bundespost has been notified that this equipment was put into circulation and was granted the right to check the product type for compliance with these requirements.

Additional Information for Test- and Measurement Equipment

Note: If test and measurement equipment is operated with unshielded cables and/or used for measurements on open set-ups, the user must insure that under these operating conditions, the radio frequency interference limits are met at the border of his premises.

Note: This declaration indicates compliance of this product with the German RFI specifications stated in the German FTZ 1046/84 directive.